In the Claims

This listing of claims will replace all prior versions, and listings, of claims.

Listing of Claims

1. (Currently Amended) A method of filling gaps between a pattern of interconnect lines forming a wiring structure on a semiconductor substrate, said interconnect lines having a top surface further having sidewalls, comprising the steps of:

providing a semiconductor substrate said substrate having a surface;

creating a network of interconnect lines on said surface of said substrate whereby said interconnect lines are separated by holes having bottoms between said interconnect lines thereby leaving said surface of said substrate partially exposed over said bottoms of said holes between said interconnect lines;

depositing a first layer of dielectric having a surface over said interconnect lines wiring structure thereby including said exposed surface of said semiconductor substrate;

performing an etch back of said first layer of dielectric thereby forming deposits of said first layer of dielectric on the top surface of the interconnect lines;

depositing a second layer of dielectric having a surface over said etched back first layer of dielectric;

etching said second layer of dielectric thereby creating exposed portions of said first layer of dielectric; and

depositing a layer of oxide over said etched second layer of dielectric thereby including said exposed portions of said first layer of dielectric.

2. (Previously presented) The method of claim 1 wherein said interconnect lines contain polysilicon.

3. (Currently Amended) The method of claim 1 wherein said interconnect lines contain a lower layer of polysilicon and an upper layer of silicon nitride (SIN) said wiring structure is applied during ~~the~~ a SAC process.

4. (Previously presented) The method of claim 1 wherein said interconnect lines contain an electrically conducting material.

5. (Original) The method of claim 1 wherein said first layer of dielectric contains High Density Plasma-oxide.

6. (Currently Amended) The method of claim 1 wherein said etch back of said first layer of dielectric is performing an etch back that is a Buffered Oxide based Etch said etch back to be performed on said first layer of dielectric thereby forming a layer of first dielectric having a surface on the bottom of the holes that separate said interconnect lines thereby further forming deposits of said first dielectric said deposits partially overlaying the top surfaces of said interconnect lines thereby creating partially exposed top corners of said interconnect lines said top corners being located at

intersects between said sidewalls of said interconnect lines and said top surface of said interconnect lines.

7. (Cancelled)

8. (Currently Amended) The method of claim [[1]] 6 wherein said depositing a second layer of dielectrie is depositing a layer of silicon nitride (Si_3N_4) said deposition covering the surface of said layer of first dielectric on the bottom of said holes between said interconnect lines thereby further covering the surface of said first dielectric partially overlaying the top surfaces of said interconnect lines thereby furthermore covering the surface of said exposed top corners of said interconnect lines.

9. (Previously presented) The method of claim 1 wherein said depositing said second layer of dielectric is depositing a layer of Si_3N_4 using PE-CVD technology at a temperature of about 400 degrees C. whereby said layer of Si_3N_4 is deposited to a thickness between about 1000 and 2000 Angstrom.

10. (Currently Amended) The method of claim [[1]] 6 wherein said depositing a second layer of dielectric is depositing a layer of aluminum oxide ($A1_30_3$) said deposition covering the surface of said layer of first dielectric on the bottom of said holes separating said interconnect lines thereby further covering the surface of said first dielectric partially overlaying the top surfaces of said interconnect lines thereby

furthermore covering the surface of the partially exposed top corners of said interconnect lines.

11. (Currently Amended) The method of claim [[1]] 6 wherein said depositing a second layer of dielectric is depositing a layer of dielectric material said deposition covering the surface of said layer of first dielectric on the bottom of the holes separating said interconnect lines thereby further covering the surface of said first dielectric partially overlaying the top surfaces of said interconnect lines thereby furthermore covering surface of the partially exposed top corners of said interconnect lines.

12. (Previously presented) The method of claim 1 wherein said etching said second layer of dielectric removing said second layer of dielectric in its totality except where said second layer of dielectric forms spacers on said sidewalls of said interconnect lines.

13. (Original) The method of claim 1 wherein said etching second layer of dielectric is etching Si_3N_4 using CHF_3 as etchant gas at a flow rate of about 15 sccm and a gas pressure of about 50 mTorr with an rf power density of about 700 watts with no magnetic field applied and an ambient wafer temperature of about 15 degrees C.

14. (Currently Amended) The method of claim [[1]] 12 wherein said depositing a layer of oxide is depositing a layer of PE-oxide or PE-TEOS (Plasma Enhanced tetraethosiloxane) over said spacers on said sidewalls of said interconnect lines thereby

furthermore depositing a layer of PE-oxide or PE-TEOS over said layer of first dielectric on the bottom of the holes between said interconnect lines thereby furthermore depositing a layer of PE-oxide or PE-TEOS over said first dielectric partially overlaying the top surfaces of said interconnect lines thereby furthermore depositing a layer of PE-oxide or PE-TEOS over the partially exposed top corners of said interconnect lines.

15. (Currently Amended) The method of claim [[1]] 14 with the additional step of planarizing said deposited layer of PE-oxide or PE-TEOS said planarization to proceed down to the plane of the top surface of said ~~conducting line~~ pattern of interconnect lines thereby completing the process of creating a high-aspect ratio pattern of ~~conducting~~ interconnect lines said ~~conducting~~ interconnect lines being separated with an Intra-Layer Dielectric.

16. (Previously presented) A method of filling gaps between a pattern of interconnect lines forming a wiring structure on a semiconductor substrate, said interconnect lines having a top-surface further having sidewalls, comprising the steps of:

providing a semiconductor substrate said substrate having a surface;

creating a network of interconnect lines on said surface of said substrate whereby said interconnect lines are separated by holes having bottoms between said interconnect lines thereby leaving said surface of said substrate partially exposed over said bottoms of said holes between said interconnect lines;

depositing a first layer of dielectric having a surface over said interconnect lines wiring structure thereby including said exposed surface of said semiconductor substrate;

performing an etch back of said a first layer of dielectric wherein said etch back is performing a Buffered Oxide Etch thereby forming a layer of first dielectric on the bottom of said holes between said interconnect lines thereby further forming deposits of said first dielectric on the top surfaces of interconnect lines said deposits partially overlaying the top surfaces of said interconnect lines thereby creating exposed top corners of said interconnect lines said top corners being located at intersects between said sidewalls of said interconnect lines and said top surface of said interconnect lines;

depositing a second layer of dielectric said deposition covering said layer of first dielectric on the bottom of said holes between said interconnect lines thereby further covering said first dielectric partially overlaying the top surfaces of said interconnect lines thereby furthermore covering the partially exposed top corners of said interconnect lines;

etching said second layer of dielectric to remove said second layer of dielectric in its totality except where said second layer of dielectric forms spacers on the sidewalls of said interconnect lines; and

depositing a layer of PE-oxide or PE-TEOS over said spacers on the sidewalls of said interconnect lines thereby furthermore depositing a layer of PE-oxide or PE-TEOS over said layer of first dielectric on the bottom of the holes

between said interconnect lines thereby furthermore depositing a layer of PE-oxide or PE-TEOS over said first dielectric partially overlaying the top surfaces of said interconnect lines thereby furthermore depositing a layer of PE-oxide or PE-TEOS over the partially exposed top corners of said interconnect lines.

17. (Previously presented) The method of claim 16 wherein said interconnect lines contain polysilicon.

18. (Previously presented) The method of claim 16 wherein said interconnect lines contain a lower layer of polysilicon and a upper layer of silicon nitride (SiN) said interconnect lines is applied during ~~the~~ a SAC process.

19. (Previously presented) The method of claim 16 wherein said interconnect lines contain an electrically conducting material.

20. (Original) The method of claim 16 wherein said first layer of dielectric contains High Density Plasma-oxide.

21. (Cancelled)

22. (Previously presented) The method of claim 16 wherein said depositing said second layer of dielectric is depositing a layer of Si_3N_4 using PE-CVD technology at a

temperature of about 440 degrees C. whereby said layer of Si_3N_4 is deposited to a thickness between about 1000 and 2000 Angstrom.

23. (Original) The method of claim 16 wherein said depositing a second layer of dielectric is depositing a layer of aluminum oxide ($A1_30_3$).

24. (Previously presented) The method of claim 16 wherein said depositing a second layer of dielectric is depositing a layer of dielectric material.

25. (Original) The method of claim 16 wherein said etching second layer of dielectric is etching Si_3N_4 using CHF_3 as etchant gas at a flow rate of about 15 sccm and a gas pressure of about 50 mTorr with an rf power density of about 700 watts with no magnetic field applied and an ambient wafer temperature of about 15 degrees C.

26. (Currently Amended) The method of claim 16 with the additional step of planarizing said deposited layer of PE-oxide or PE-TEOS said planarization to proceed down to the plane of the top surface of said ~~conducting line~~ pattern of interconnect lines thereby completing the process of creating a high-aspect ratio pattern of ~~conducting~~ interconnect lines said ~~conducting~~ interconnect lines being separated with an Intra-Layer Dielectric.